REMARKS

Claims 1-16 were pending in the application. Claim 15 was rejected under 35 U.S.C. §102(b) as being anticipated by Radogna et al (hereinafter "Radog"). Claims 1-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Radog and Latif et al. Claims 14 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Radog and Latif as applied to claims 1 and 15, and further in view of Muller et al. Claim 3 has been canceled in this response (and claims 17-23 were previously canceled without prejudice), leaving claims 1, 2 and 4-16 presently pending in the application. Claims 1, 5, 6 and 15 have been amended. Reconsideration and reexamination of the application in view of the amendments and following remarks is respectfully requested.

Claims 1 and 15 have been similarly amended to recite, in part (with forward slashes // indicating the differences in language between claims 1 and 15):

> an instruction memory accessible to /the at least one microsequencer of the microsequencer system//said processing element/, said instruction memory having a plurality of instruction words, each of said instruction words forming a Very Long Instruction Word (VLIW) having a plurality of instruction fields executable in parallel by different functional units of /each at least one microsequencer//the processing element/ to enable the /at least one microsequencer//processing element/ to execute a plurality of instructions in a single instruction cycle.

Support for the amendments to claims 1 and 15 can be found on page 9 lines 16-19, page 18 lines 18-28, and FIGs. 7 and 8. In addition, because all of the other presently pending claims depend from claims 1 and 15, all of the pending claims now contain the limitation shown above.

Claim 15 was rejected under 35 U.S.C. §102(b) as being anticipated by Radog. With the amendment to claim 15, it is respectfully submitted that this rejection has been overcome.

The present invention is directed to enabling data communication between a storage area network and another network implementing different protocols. At least one microsequencer system is employed to perform a translation between the two different protocols. The microsequencer system may include two or more microsequencers connected together to perform the translation using Very Long Instruction Words (VLIW) from an instruction memory for processing multiple

instructions in parallel. Each VLIW contains a plurality of instruction fields executable in parallel by different instruction units within the microsequencer.

Radog fails to disclose *a VLIW with a plurality of executable instruction fields*, as recited in amended claim 15. In his rejection of original claim 15, the Examiner cites col. 6 lines 41-47 of Radog as disclosing an instruction memory containing a plurality of instruction words, each having sufficient length to hold at least two instructions. Although claim 15 has since been amended, it should be understood that Radog only discloses "longwords" loaded in THV0 and THV1 registers (see col. 6 lines 41-46), the contents of which are illustrated in FIGs. 5a and 5b. However, FIGs. 5a and 5b clearly illustrate that these "longwords" stored in THV0 and THV1 *do not contain a plurality of executable instruction fields* at all – rather, they merely comprise parameters and control information necessary for the translation of a header.

The present amendments to claim 15 further distinguish Radog. Radog contains no disclosure at all related to *parallel processing of a VLIW by different instruction units within a microsequencer*, as recited in amended claim 15. Note that examples of these instruction units include a translate block 74, a data verification block 70, and the adder 68 shown in FIG. 8 of the application and described on page 18 lines 22-26. In contrast, Radog merely discloses a separate processor 46 or 60 in either the receive or transmit path for translating receive headers and transmit headers, but fails to mention or show any ability of these processors to perform parallel processing using different instruction units (processing elements) within a microsequencer.

Because Radog does not disclose, teach or suggest the parallel processing of multiple executable instruction fields of a VLIW by different instruction units within a microsequencer, Radog cannot perform a plurality of instructions in a single instruction cycle and cannot realize the processing improvements in the manner achievable by the present invention.

Because Radog does not disclose all of the limitations of amended claim 15, it is respectfully submitted that the rejection of claim 15 under 35 U.S.C. §102(b) as being anticipated by Radog has been overcome.

Claims 1-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Radog and Latif. Claim 3 has been canceled, rendering the rejection of that claim moot. With the amendment to claim 1, it is respectfully submitted that the rejection of claims 1, 2 and 4-13 has been overcome.

As mentioned above, amended claims 1 and 15 now contain the same limitation (the parallel processing of multiple executable instruction fields of a VLIW by different instruction units within a microsequencer). Also demonstrated above with regard to claim 15 is Radog's failure to disclose this limitation. Therefore, Radog also fails to disclose this limitation in claim 1. Furthermore, Latif fails to make up for the deficiencies of Radog, in that Latif is also completely silent with regard to the parallel processing of multiple executable instruction fields of a VLIW by different instruction units within a microsequencer.

Because neither Radog nor Latif discloses, teaches or suggests all of the limitations of amended claim 1, it is respectfully submitted that the rejection of claim 1 under 35 U.S.C. §103(a) as being unpatentable over Radog and Latif has been overcome. In addition, because claims 2 and 4-13 depend from claim 1, the rejection of those claims has been overcome for the same reasons provided above with respect to claim 1.

Claims 14 and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Radog and Latif as applied to claims 1 and 15, and further in view of Muller. With the amendments to claims 1 and 15, it is respectfully submitted that this rejection has been overcome.

Claim 14 depends from amended claim 1, and claim 16 depends from amended claim 15. As demonstrated above, neither Radog nor Latif discloses, teaches or suggests all of the limitations of amended claim 1, in particular the parallel processing of multiple executable instruction fields of a VLIW by different instruction units within a microsequencer. Furthermore, because amended claim 15 now contains this same limitation, it can also be said that neither Radog nor Latif discloses, teaches or suggests all of the limitations of amended claim 15. Muller also fails to make up for the deficiencies of Radog and Latif, in that Muller is also completely silent with regard to the parallel

processing of multiple executable instruction fields of a VLIW by different instruction units within a microsequencer.

Because neither Radog nor Latif nor Muller discloses, teaches or suggests all of the limitations of amended claims 1 and 15, it is respectfully submitted that the rejection of claims 14 (which depends from claim 1) and 16 (which depends from claim 15) under 35 U.S.C. §103(a) as being unpatentable over Radog and Latif and in further view of Muller has been overcome.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If, for any reason, the Examiner finds the application other than in condition for allowance, Applicants request that the Examiner contact the undersigned attorney at the Los Angeles telephone number (213) 892-5752 to discuss any steps necessary to place the application in condition for allowance.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicants petition for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Docket No. 491442004500.

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Respectfully submitted,

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